AMENDMENT TO THE SPECIFICATION:

Please amend page 12, lines 6-22 as follows:

Fig. ~~5~~ 6 is a block diagram of an exemplary timing recovery device 470 with a controller 610, a memory 620, a filter device 625, a channel device 630, a noise device 640, a matrix device 650, a forward-time device 660, a time-reverse device, a selector 680, an input interface 710 and an output interface 720. The controller 610 interfaces with the other components 620-720 using a control/data bus 602. Although the exemplary timing recovery device 470 uses a bussed architecture, it should be appreciated that the exemplary timing recovery device 470 can use any known or later developed architecture such as an array of electronic circuits such as a combination of PALs, PDAs, FPGAs and the like.

Please amend page 16, line 28 to page 17, line 2 as follows:

In step ~~1100~~ 1110, a determination is made whether to continue to receive further communication signals. If further communication signals are to be received, control jumps back to step 1010 where a next communication signal is received; otherwise, control continues to step 1120 where the process stops.